A Novel Intermediate Bus Converter Topology for Cutting Edge Data Center Applications

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Abstract: As new technologies emerge data centers and servers have established themselves as one of the largest and fastest growing consumers of power. While switched capacitor converter topologies have some very attractive features, namely low reliance on magnetic components and high efficiency, several critical factors have prevented their adoption in high current data center applications. The family of converters proposed are novel intermediate bus converter that demonstrates the highest performance yet achieved for 48 V to 12 V conversion with up to 2.5 kW/in^3 power density, higher than 99% peak efficiency, and 97.2% full load efficiency for 12 V/70 A output. The reduction of voltage stress across the MOSFETs as well as extremely low reliance on magnetics are the key driving factors behind this high efficiency and power density, and are achieved without a sensitive resonant design or the usage of complex control technique.

Keywords: DC-DC converter, data centers, intermediate bus architecture

1 Introduction

Cutting edge data centers have transitioned from traditional 12 V distribution to the server rack to a higher 48 V distribution. This offers several advantages in terms of upstream distribution losses, and substantially reduced transmission losses, but does present a challenge at the point of load where voltages as low as 0.8 V at currents above 1 000 A can be required. This extremely high step-down ratio is very challenging for conventional converter topologies, and a two-stage conversion approach is generally utilized such as the intermediate bus architecture (IBA). In this architecture an "intermediate bus" converter will convert the 48 V down to some lower voltage, typically around 12 V, and a second point of load converter will then convert that 12 V down to the 0.8 V required by the load, while also providing regulation.

Switched capacitor converters have seen a recent resurgence of research interest, particularly aimed at next generation data center power architectures. Advances in semiconductor switches, as well as a relative lack of improvement in bulky magnetic components, have made DC-DC converters with a lower reliance on magnetics a particularly attractive option where high power density and efficiency are required. Switched capacitor converters can, in theory, eliminate these large magnetic components. Additionally, switched capacitor converters operate optimally at fixed integer conversion ratios (such as 4:1 stepdown for 48 V to 12 V conversion). In an IBA where regulation is not required for the bus converter, this makes switched capacitor converters an extremely attractive option. As shown in Fig. 1 [1], which presents a comparison of several 48 V to 12 V converter designs, in applications where regulation is not required, unregulated converters can provide an extremely large advantage in terms of both efficiency and power density when compared with regulated converter options.

However, conventional switched capacitor converter topologies have several practical limitations that can prevent their wide adoption for high current/power level applications. The zero inductor-voltage (ZIV) converter is a converter that maintains the key advantages offered by switched capacitor converters, namely extremely low reliance on magnetic components, without any of the drawbacks traditionally associated with switched capacitor converters operating at high current levels. The ZIV

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converter has achieved the highest power density and efficiency yet demonstrated in literature for an unregulated, 48 V to 12 V intermediate bus converter. As shown in Fig. 1, the two phase 12-switch ZIV converter achieves 2.5 kW/in^3 power density for 48 V to 12 V conversion at 70 A load current with a full load efficiency of 97.2%.

This paper is organized as follows. Section 2 will present an overview of existing switched capacitor converters for IBA. Section 3 will present the ZIV converter family. Section 4 will present simulation results and analysis related to the ZIV converters. Section 5 will present the experimental results, and Section 6 will conclude the paper.

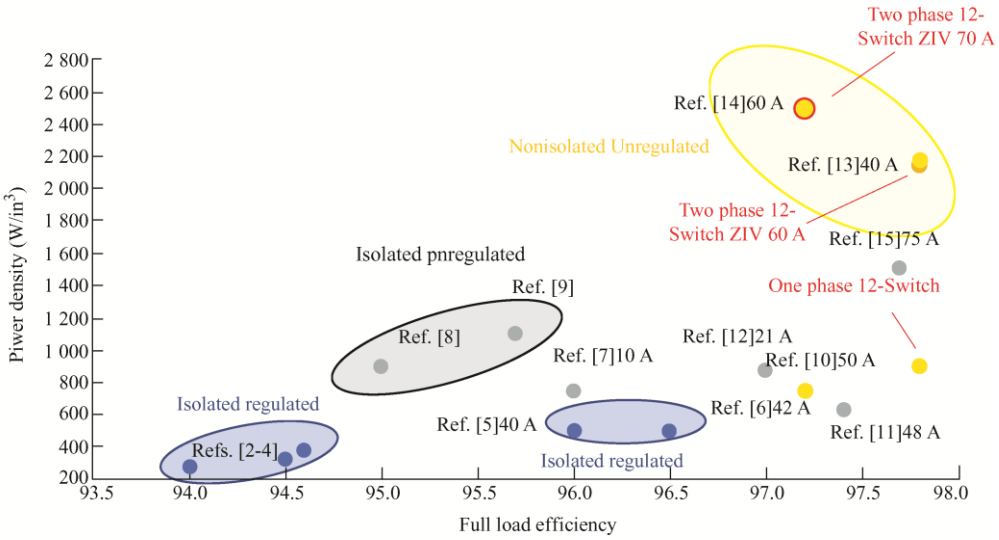

Fig. 1 Comparison of converter topologies for 48 V to 12 V conversion

2 Overview of switched capacitor topologies for intermediate bus applications

In conventional switched capacitor converter (SCC) topologies it generally not possible to regulate the output voltage without introducing significant loss. The optimal operating point will typically occur at an integer-ratio step-down as determined by the circuit topology. While this may preclude their use in certain applications in the intermediate bus architecture it is possible for the intermediate bus converter to operate as a so-called DC-transformer (DCX), and output voltage regulation is not required. Switched capacitor converters have therefore become widely researched for these DCX applications in datacenters. Additionally, in many conventional DC-DC converter topologies the magnetic components are the largest components and are lossy. Switched capacitor converters aim to remove, or at least significantly reduce, the need for any magnetic components in the converter to achieve much higher power densities, and efficiencies than conventional topologies [16].

In conventional switched capacitor converter topologies, however, there is a fundamental issue with a true magnetics-less SCC, namely the charge redistribution loss. This charge redistribution loss occurs when a low impedance switch is closed between two paralleled capacitors and results in a current spike, as shown in Fig. 2, as well as energy loss associated with charge redistribution. To reduce this loss and limit the current spike, larger capacitors or higher switching frequencies are required than would otherwise be desired, reducing both the power density and efficiency advantages offered by SCC topologies.

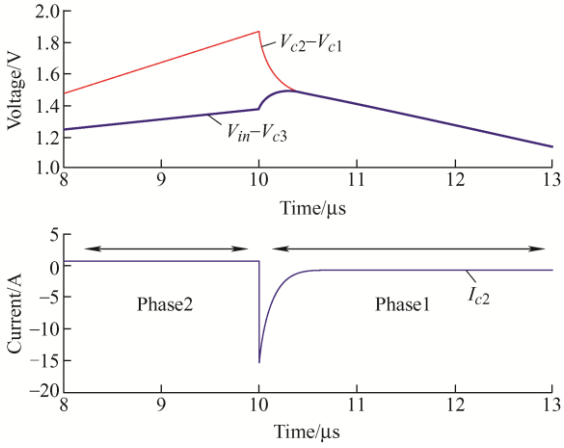

Fig. 2 4:1 Dickson SCC example capacitor current spike, caused by parallel connection of mis-matched flying capacitors [17]

In order to address the charge redistribution problem, SCCs with added inductive elements,

sometimes referred to as hybrid SCC topologies, have been proposed. Many such topologies have been derived, utilizing the principle that adding an inductive element between the two paralleled capacitors will eliminate the charge redistribution current spike and associated loss [18].

However, many of these designs are not suitable for high volume applications such as data centers for several critical reasons. First, immunity to component non-idealities is crucial. Ceramic capacitors and off-the-shelf inductors typically have fairly large component tolerances (>10%), along with the DC-voltage derating and effects of temperature on ceramic capacitors, it is impossible to guarantee that precisely tuned resonant circuits relying on these components can be mass produced. Scalability to different power levels is also critical. In order to achieve this, it should be possible to parallel the intermediate bus converters with reasonably good current sharing performance. Scalability of control is also a concern; utilizing techniques that require additional sensing can cause issues with paralleling or scaling to differing power levels.

3 Zero inductor-voltage converter family

The technical approach used in this paper is different from the above-mentioned SCC converter with inductor as a current limit component. The converter topology proposed in this paper is a PWM switching converter that can (1) include an inductor, (2) operate at PWM mode, and (3) make zero voltage across the inductor. In this ZIV topology the voltage across the inductor is independent of the input and output voltages. The inductor voltage is the ripple voltage of the input capacitor, output capacitor and flying capacitor. The capacitors in this topology are always connected in series, never in parallel. The voltage blocking of the flying capacitors also reduces the voltage stress of the MOSFETs. Since it is derived from a PWM converter, the operation of the converter is not sensitive to the capacitor or inductor value tolerance. As a result, the design of this converter is greatly simplified, and extremely good efficiency and power density can be achieved as will be shown in Section 5.

3.1 Proposed 7-switch zero inductor-voltage converter

The ZIV converter utilizes 7 MOSFETs and 2 flying capacitors in the topology shown in Fig. 3 [19]. The PWM gate drive signals are shown in Fig. 4. From this, it can be observed that the converter has 3 operating states, labelled *A*, *B* and *C*. The equivalent circuit for each operating state is shown in Fig. 5. In operating state *A*, MOSFETs *M*1, *M*3 and *M*6 are on. In this state the flying capacitors are being charged. In operating state *B*, MOSFETs *M*1 and *M*3 are turned off, *M*2 and *M*4 are turned on, and *M*6 remains on. The first flying capacitor, C_{f1} is now being discharged, while C_{f2} continues to charge. In operating state *C*, all the first stage MOSFETs (*M*1-*M*4) are now turned off. MOSFET *M*6 is turned off, and MOSFETs *M*5 and *M*7 are turned on. C_{f1} is now disconnected and does not carry any current during this operating state, while C_{f2} is discharged for the remainder of the switching period.

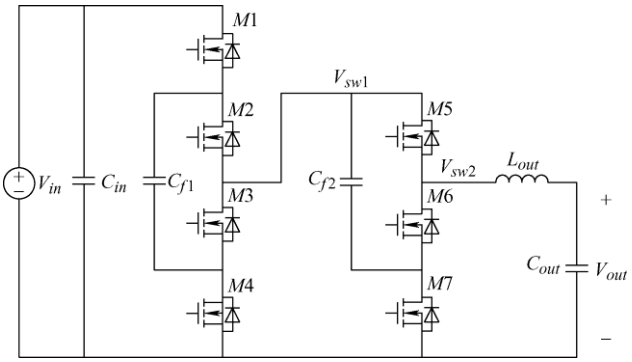

Fig. 3 7-switch ZIV converter topology

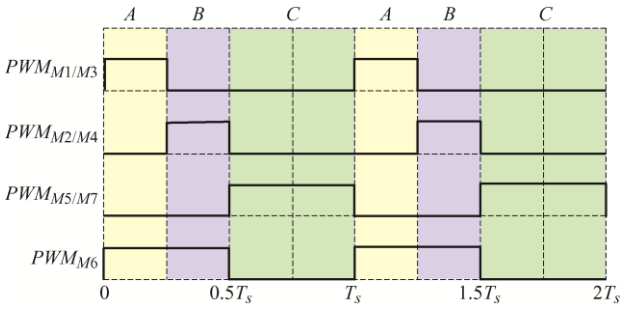

Fig. 4 7-switch ZIV converter PWM gate signal diagram

From these figures the flying capacitors are never placed in parallel, and the inductor is always in the current path. This means that there is no current spike of the capacitors; soft-charging is an inherent feature of the topology and does not depend on any particular component tolerances, or additional inductors added to the current carrying branches. The key drawback of the 7-switch ZIV topology is that the first-stage MOSFETs (*M*1-*M*4) operate with only 25% duty cycle. It is desirable to operate MOSFET pairs with 50% duty cycle to achieve full utilization of the switching devices.

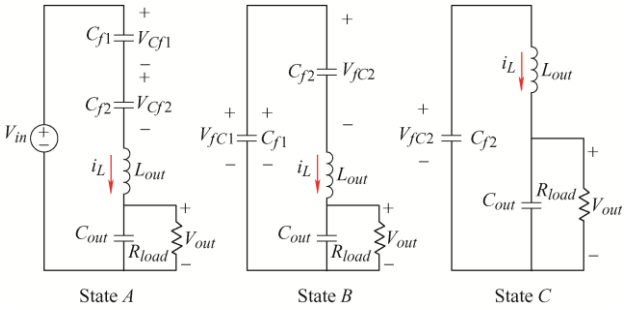

Fig. 5 Equivalent circuits in operating states *A*, *B* and *C*

3.2 Proposed 12-switch ZIV converter

In order to address the issue of the MOSFET utilization, the 12-switch ZIV converter topology shown in Fig. 6 [20].

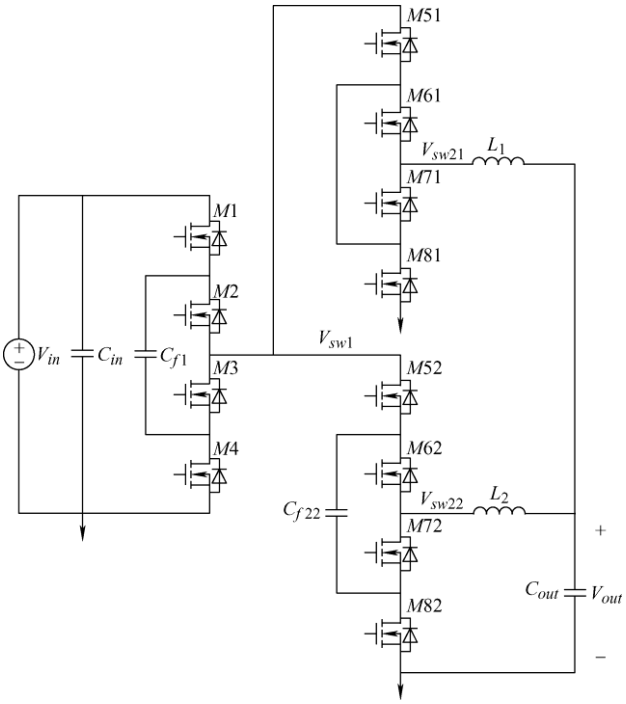

Fig. 6 Proposed 12-switch ZIV converter topology

This converter utilizes two paralleled second-stages but requires only one input-stage. This results in significant component and size savings compared with a two-phase 7-switch ZIV converter, while also offering greatly improved efficiency and power density when compared with a single-phase 7-switch ZIV converter. The operation of this topology, and the realization of the component reduction, is best understood by examining two single-phase ZIV converters operating in parallel with a 180-degree phase shift. Note that for each phase, the first stage switches *M*1-*M*4 will be off for 50% of the total converter cycle during State *C* (from $0.5T_s$ to T_s, $1.5T_s$ to $2T_s$, etc) as shown in Fig. 4. Fig. 7 shows the PWM gate drive diagram for the 12-switch ZIV converter.

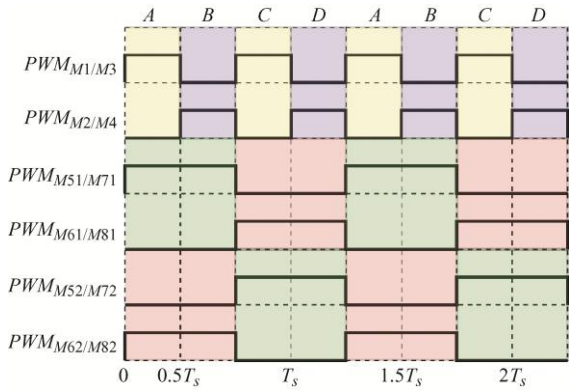

Fig. 7 12-switch ZIV converter topology PWM gate drive diagram

3.3 Steady state operation

Note that the following derivation will be presented for the 7-switch ZIV converter. The analysis for the 12-switch ZIV converter is identical, with the understanding that States *C* and *D* (Fig. 7) are exactly mirrored to states *A* and *B*.

In order to understand the 4:1 step down ratio provided by this converter topology the inductor voltage can be analyzed in the steady state where V_{LA} is the inductor voltage in State *A*, V_{LB} is the inductor voltage in State *B*, V_{LC} is the inductor voltage in State *C*, $V_{Cf1\text{-}A}$ and $V_{Cf2\text{-}A}$ are the two flying capacitor voltages in State *A*, $V_{Cf1\text{-}B}$ and $V_{Cf2\text{-}B}$ are the two flying capacitor voltages in State *B*, and $V_{Cf2\text{-}C}$ is the second flying capacitor voltage in State *C*.

$$\text{State } A\text{: } V_{LA} = V_{in} - V_{Cf1\text{-}A} - V_{Cf2\text{-}A} - V_{out} \tag{1}$$

$$\text{State } B\text{: } V_{LB} = V_{Cf1\text{-}B} - V_{Cf2\text{-}B} - V_{out} \tag{2}$$

$$\text{State } C\text{: } V_{LC} = V_{Cf2\text{-}C} - V_{out} \tag{3}$$

As seen from the gate signal diagram, Fig. 4, State *A* is active for 25% of one switching cycle, State *B* is active for 25% of one switching cycle, and State *C* is active for the remaining 50% of the switching cycle. Thus the average inductor voltage over one switching cycle can be expressed as

$$V_L = \frac{V_{LA}}{4} + \frac{V_{LB}}{4} + \frac{V_{LC}}{2} \tag{4}$$

Note that the capacitor charge balance must also be maintained for steady state operation. This means that the average voltage of C_{f1} in State *A* must be equal

to the average voltage of C_{f1} for State *B*, as C_{f1} is charged for 25% of the switching cycle in State *A*, discharged for 25% of the switching cycle in State *B*, and is disconnected in State *C*

$$V_{Cf1\text{-}A} = V_{Cf1\text{-}B} \tag{5}$$

For C_{f2} the average voltage of C_{f2} across both States *A* and *B* must be equal to the average voltage of C_{f2} across State *C*. This is because C_{f2} is charged for 25% of the switching cycle in State *A*, continues to be charged for an additional 25% of switching cycle in State *B*, and then is discharged for the remaining 50% of the switching cycle in State *C*

$$\frac{V_{Cf2\text{-}A} + V_{Cf2\text{-}B}}{2} = V_{Cf2\text{-}C} \tag{6}$$

Substituting Eqs. (1), (2) and (3) into Eq. (4) with the equivalencies noted in Eqs. (5) and (6) gives

$$V_L = \frac{V_{in}}{4} - (0) - (0) - V_{out} = 0 \tag{7}$$

Under steady state operation the average inductor voltage across one switching cycle must be zero, and utilizing the equivalencies given in Eqs. (5) and (6) the capacitor voltage terms cancel out as shown in Eq. (7) leaving

$$V_{out} = \frac{V_{in}}{4} \tag{8}$$

Thus, the ZIV converter family as presented provides a fixed 4:1 stepdown ratio under steady-state operation.

3.4 ZIV operation

As mentioned in Section 1 the ability to reduce the reliance on large magnetic components is the critical advantage allowing SCC topologies to achieve high power density and efficiency. While the ZIV converter is not an SCC topology, and thus avoids the critical drawbacks such as charge redistribution, it does maintain the advantage of very low reliance on magnetic components. This can be understood by examining the voltage at V_{sw2} in Fig. 3.

The first flying capacitor will have a nominal DC value of 0.5 V_{in}, and the second flying capacitor will have a DC value of 0.25 V_{in} nominally. These capacitor voltages can be expressed as a nominal DC value, summed with a ripple voltage.

$$V_{Cf1} = \frac{V_{in}}{2} + v_{Cf1rip} \tag{9}$$

$$V_{Cf2} = \frac{V_{in}}{4} + v_{Cf2rip} \tag{10}$$

For State *A*

$$v_{n2} = V_{in} - v_{Cf1} - v_{Cf2} \tag{11.1}$$

$$v_{n2} = V_{in} - \frac{V_{in}}{2} - \frac{V_{in}}{4} - v_{Cf1rip} - v_{Cf2rip} \tag{11.2}$$

$$v_{n2} = \frac{V_{in}}{4} - v_{Cf1rip} - v_{Cf2rip} \tag{11.3}$$

For State *B*

$$v_{n2} = v_{Cf1} - v_{Cf2} \tag{12.1}$$

$$v_{n2} = \frac{V_{in}}{2} - \frac{V_{in}}{4} + v_{Cf1rip} - v_{Cf2rip} \tag{12.2}$$

$$v_{n2} = \frac{V_{in}}{4} + v_{Cf1rip} - v_{Cf2rip} \tag{12.3}$$

For State *C*

$$v_{n2} = v_{Cf2} \tag{13.1}$$

$$v_{n2} = \frac{V_{in}}{4} + v_{Cf2rip} \tag{13.2}$$

For all of the above states, the voltage at V_{sw2} is equal to 0.25 V_{in} plus the capacitor ripple voltage. The inductor is connected between V_{sw2} and the output voltage, which is also shown to be equal to 0.25 V_{in}. Thus, the only voltage seen by the inductor will be due to the capacitor voltage ripple. This means the inductor voltage is independent of the input and output voltage level. Therefore, a very small inductor can be used to achieve acceptable inductor ripple. The low inductor voltage stress means that very small inductors, as small as 100 nH, can be utilized even with switching frequencies below 100 kHz.

4 Analysis and computer simulation

4.1 Loss analysis

Loss analysis is conducted for the 7-switch ZIV converter. Tab. 1 shows the components used in the 7-switch ZIV converter design.

Tab. 1 7-switch ZIV converter loss analysis components

Component	Part number	Key parameters
First stage MOSFETs (*M*1-*M*4)	BSC011N03LSI	R_{ds}=1.1 mΩ Q_g=20 nC
Second stage MOSFETs (*M*5-*M*7)	BSC009NE2LS5I	R_{ds}=0.95 mΩ Q_g=17 nC
Inductor	SLR1075-231	*L*=230 nH *DCR*=0.29 mΩ
Flying capacitor C_{f1}	10×10 µF Ceramic	*ESR*=1.5 mΩ
Flying capacitor C_{f2}	10×47 uF Ceramic	*ESR*=0.75 mΩ
Input capacitor	10×10 µF Ceramic	*ESR*=1.5 mΩ

The conduction losses for the MOSFET, inductors and capacitors are estimated straightforwardly by Eq. (14). Note that the inductor loss, for the ZIV converter, is entirely winding loss as any core loss will be negligible.

$$P_{cond} = I_{RMS}^2 R \tag{14}$$

The switching loss for the MOSFETs is estimated according to Eq. (15) where t_{on} is the turn-on time of the MOSFET, and t_{off} is the turn-off time of the MOSFET.

$$P_{sw} = \frac{1}{2} V_{ds} I \left(t_{on} + t_{off} \right) f_{sw} \tag{15}$$

The deadtime (MOSFET body diode) loss is estimated according to Eq. (16) where $t_{dt\text{-}r}$ is the rising edge dead time and $t_{dt\text{-}f}$ is the falling edge deadtime and V_{sd} is the reverse diode voltage of the MOSFET.

$$P_{dt} = V_{sd} I \left(t_{dt\text{-}r} + t_{dt\text{-}f} \right) f_{sw} \tag{16}$$

The gate drive loss is estimated according to Eq. (17).

$$P_{gate} = Q_g V_{gs} f_{sw} \tag{17}$$

The loss analysis was performed for an input voltage of 48 V, and a load current of 25 A with a switching frequency of 60 kHz and the results are shown in Fig. 8. Note that under this load condition the conduction loss makes up over 80% of the total converter loss, despite being a hard-switched topology that does not rely on a resonant design.

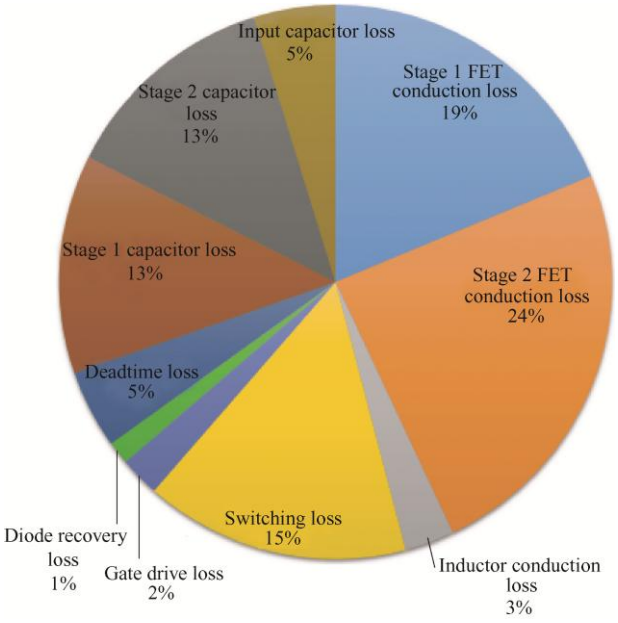

Fig. 8 7-switch ZIV converter loss analysis (25 A load, 60 kHz switching frequency)

4.2 Inductor voltage analysis

Using the same components outlined in Tab. 1 in a computer simulation the inductor voltage was analyzed to verify the "zero inductor-voltage" operation of the converter. The results of the simulation for 25 A load and 60 kHz switching frequency are shown in Fig. 9.

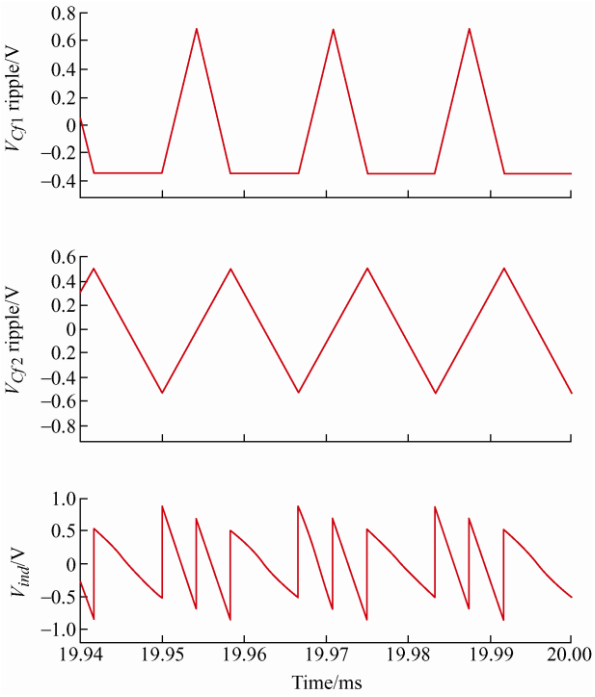

Fig. 9 Simulated capacitor voltage ripple and inductor voltages 25 A load 60 kHz switching frequency

From this simulation it is confirmed that the inductor sees only the capacitor ripple voltages, resulting in a very low overall reliance on magnetic components.

4.3 Current sharing analysis

As mentioned in Section 2, scalability to differing power levels is a crucial consideration for intermediate bus converter topologies and this is commonly achieved through the paralleling of multiple phases of converters. In the case of the ZIV converter, the current sharing can be achieved passively through the output voltage "droop" characteristic inherent to the ZIV converter.

In the ideal case, with lossless switches, the ZIV converter would be expected to output a voltage equal to exactly one-quarter of the input voltage. In practice the converter output will be slightly lower than the

expected value of 0.25 V_{in}. This is caused by the conduction related voltage drop across the components of the converter, such as the MOSFETs, inductors, flying capacitors and PCB traces. As this voltage drop will be linearly proportional to the load current the output voltage of the ZIV converter can be modelled by the following equation

$$V_{out} = V_{out\_NL} - I_{out} R_{out} \tag{18}$$

If two ZIV converters are connected in parallel, then the current carried by each phase will be determined according to the output voltage characteristic of each phase. If R_{out1} and R_{out2} are the lump equivalent resistance for each phase of the ZIV converter then the current sharing is given by

$$I_{out1} = I_{out} \frac{R_{out2}}{R_{out1} + R_{out2}} \tag{19}$$

$$I_{out2} = I_{out} \frac{R_{out1}}{R_{out1} + R_{out2}} \tag{20}$$

Fig. 9 demonstrates a case where the resistance value of phase 2 (comprised primarily of the MOSFET $R_{ds(on)}$ and capacitor *ESR*) is 10% higher than the lump resistance of phase 1. Note that in Fig. 9 the output current is give as the per-phase value, therefore 35 A per phase current would represent a total full load current of 70 A. For a 50 A total load with 10% resistance increase in one phase relative to the other, the output voltage will be approximately 11.73 V for 48 V input. The current will share according to the equations

$$I_{ph1} = 26.2\ \text{A} = 25\ \text{A} + 4.8\% \tag{21}$$

$$I_{ph2} = 23.8\ \text{A} = 25\ \text{A} - 4.8\% \tag{22}$$

The modelled output voltage characteristic is derived from the components in Section 5, Tab. 3 and shown in Fig. 10. Using these components, the output voltage for the ZIV converter design would be 11.73 V at 50 A load current. The first phase would carry 26.2 A of the load. The second phase would carry 23.8 A of the load. As demonstrated here, the droop output voltage characteristic cannot guarantee perfect current sharing. Manufacturing tolerances and component-to-component variation will result in some current sharing mismatch in a multi-phase ZIV converter design. However, as this analysis shows, the passive current sharing will offer reasonably good performance. This means scalability to differing power levels can be achieved without added control complexity. In addition, the phase which carries higher current will become hotter and therefore, the R_{ds} of the MOSFET for that phase will be increased, which will further improve the current sharing between the phases.

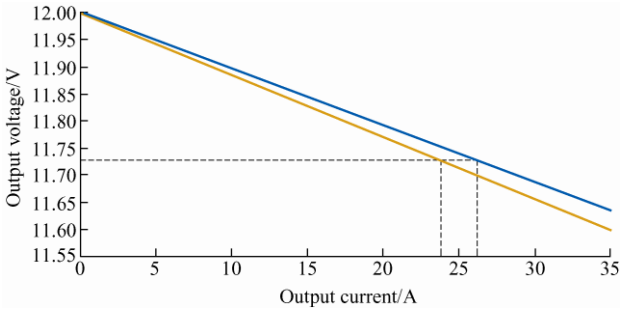

Fig. 10 Two-phase ZIV converter per-phase output voltage with 10% equivalent resistance mis-match

5 Experimental results

Experimental results are presented for a 7-switch ZIV converter design, and a two-phase 12-switch ZIV converter design. The 7-switch ZIV converter represents a proof of concept design, and demonstrates the very high efficiency of the ZIV converter, while the two-phase 12-switch ZIV converter design is optimized to achieve extremely high power density, while also demonstrating that the ZIV converter can be easily scaled to higher power levels through paralleling.

5.1 7-switch ZIV converter prototype

A prototype was constructed using the components outlined in Tab. 2. The experimental results presented in this section were gathered with an input voltage of 48 V, a switching frequency of 60 kHz, and a nominal load current of 25 A.

Tab. 2 7-switch ZIV converter prototype components

Experimental prototype components	Value/part number
Input capacitor C_{in}	16×4.7 μF 100 V X7S 1210
First flying capacitor C_{f1}	14×10 μF 50 V JB 1206
Second flying capacitor C_{f2}	10×47 μF 25 V X5R 1210
Output capacitor C_{out}	10×47 μF 25 V X5R 1210
*M*1-*M*4	30 V BSC011N03LSI
*M*5-*M*7	25 V BSC009NE2LS5I
Inductor	230 nH SLR 1075-231KE
Switching frequency f_{sw} / kHz	60

Fig. 11 shows a photograph of the top side of the converter prototype, with the key components labelled. The driver circuitry, as well as additional capacitors are located on the back of the prototype. The prototype has a width of 0.9 in, length of 1.3 in and a height of 0.45 in giving an overall power density for 12 V 35 A output of 800 W/in^3.

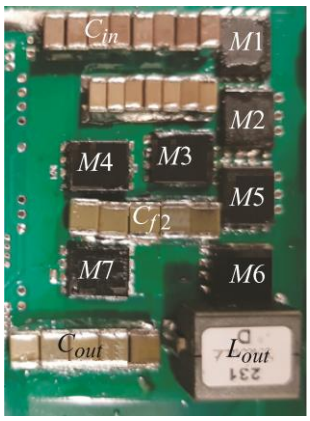

Fig. 11 7-switch ZIV converter prototype top-side photograph

Fig. 12 shows the converter input voltage, the voltage of the two flying capacitors and the output voltage. For the 48 V input voltage the flying capacitor charges to $0.5V_{in}$ or 24 V, the second flying capacitor charges $0.25V_{in}$ or 12 V, and the output voltage is also $1/4V_{in}$ or 12 V.

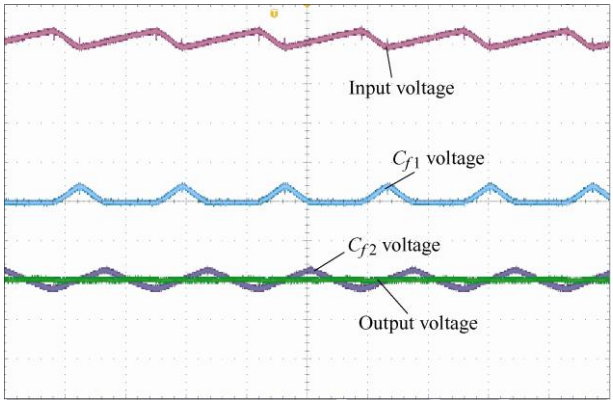

Fig. 12 Converter input voltage, C_{f1} voltage, C_{f2} voltage, output voltage

Fig. 13 shows the inductor current (top) and inductor voltage (bottom) waveforms. The shapes of the inductor current and voltage waveforms closely match the results expected from the simulation. The practical ZIV converter requires deadtime between switching transitions to prevent shoot-through. This can be seen in Fig. 13, as the inductor sees a negative voltage during this deadtime. However, the deadtime in the circuit is extremely short, at around 10 ns.

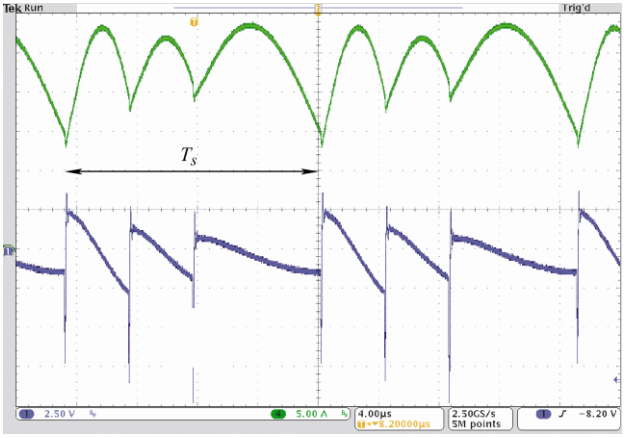

Fig. 13 Inductor current (top) and inductor voltage (bottom) waveforms 25 A load

Therefore the impact of this deadtime on the overall inductor current ripple is almost negligible. The start-up waveform for the converter prototype is shown in Fig. 14, with the input voltage, C_{f1} and C_{f2} voltages presented. It should be noted that no active capacitor balancing or control circuitry is added to the circuit, therefore, this procedure also validates that the capacitors will naturally balance near their expected value based on the duty cycle of the MOSFETs, as the capacitors naturally correct for the "imbalance" created when the input voltage is stepped, and quickly settle to their nominal values of $0.5V_{in}$ and $0.25V_{in}$ respectively. This also means no additional control complexity is required to balance the capacitors in the ZIV converter.

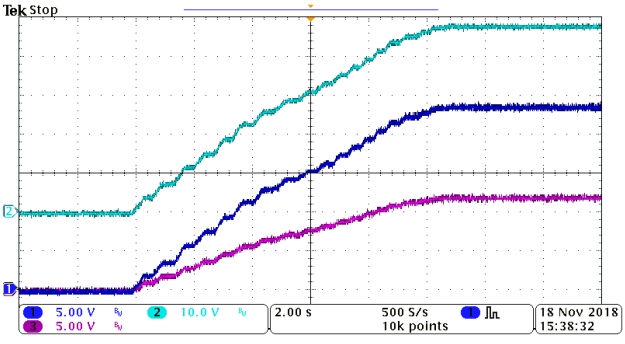

Fig. 14 Input voltage, C_{f1} and C_{f2} start-up voltage waveforms

Fig. 15 shows the measured prototype efficiency (including gate-drive loss) using Reidon *RSN* series (0.1% error) current shunts as well as a Keithley 2 700 digital multimeter. A small USB desk fan is used to cool the prototype. With a more powerful fan, or additional heat sinking, a higher load current could have been achieved as the inductor saturation current is 49 A.

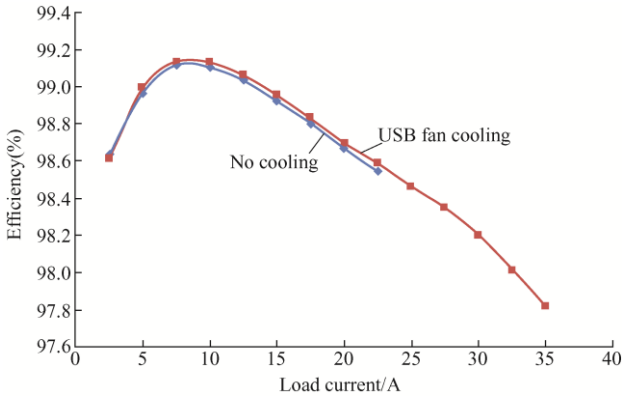

Fig. 15 Measured 7-switch ZIV converter efficiency including gate-drive loss

In order to validate the theoretical current sharing analysis two phases of the ZIV converter design were operated in parallel. The ripple voltages of each flying capacitor were measured to approximate the current carried by each phase. The flying capacitor ripples for Phase 1 is shown in Fig. 16, and Phase 2 is shown in Fig. 17. As shown by these figures the current is shared approximately equally, with no additional active control. An experiment was conducted using 20 V input (5 V output) where the load current was stepped from 1 A to 20 A, and back down to 1 A. The V_{out} dynamic response to this load transient is presented in Figs. 18 and 19. The current slew rate was 10 A/μs (the maximum possible for the testing equipment).

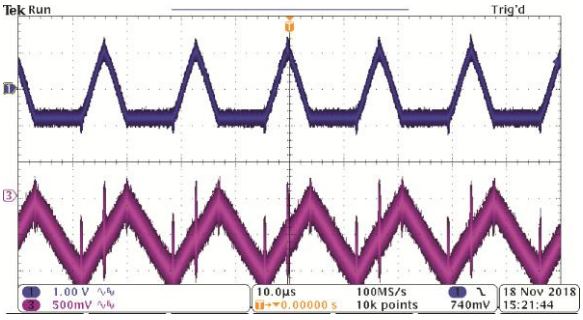

Fig. 16 Phase 1 C_{f1} and C_{f2} ripple voltage waveforms (30 A load)

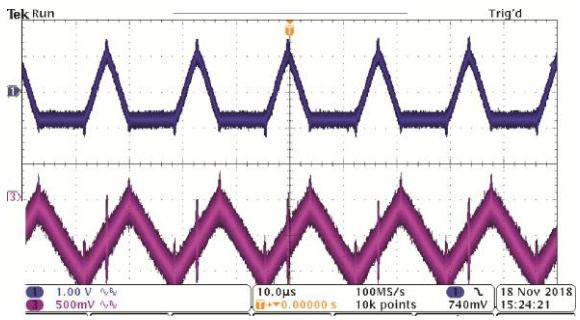

Fig. 17 Phase 1 C_{f1} and C_{f2} ripple voltage waveforms (30 A load)

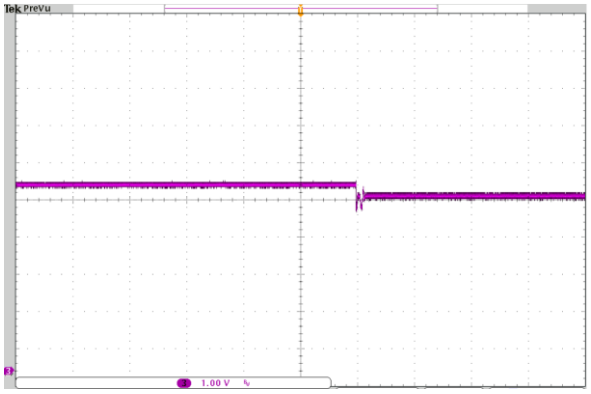

Fig. 18 V_{out} dynamic response 1 A to 20 A load step

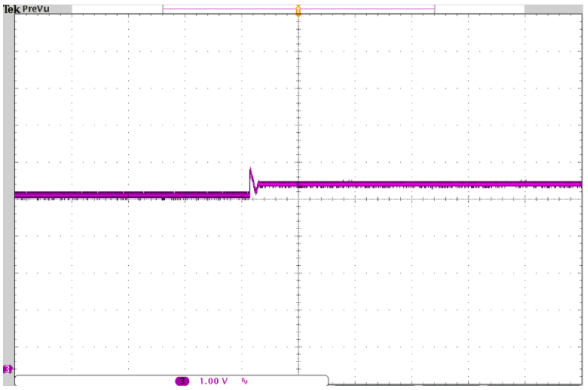

Fig. 19 V_{out} dynamic response 20 A to 1 A load step

5.2 Two-phase 12-switch ZIV converter prototype

This experimental results section focuses on a two-phase design of the 12-switch ZIV converter. While the 7-switch design was intended to verify the functionality of the topology, the two-phase 12-switch ZIV design allows for significant power density improvements to be made. Fig. 20 shows a photo of the power stage (top) and driver circuitry (bottom) for one phase of the converter. The dimensions for one phase of the converter design are 1 in×0.75 in×0.226 in (25.4 mm×19.1 mm×5.7 mm). Tab. 3 shows the components selected for the experimental prototype.

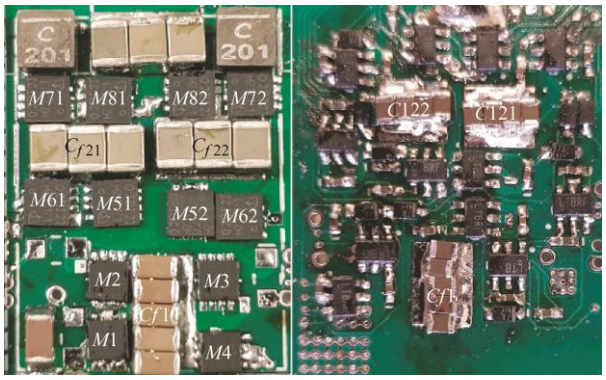

Fig. 20 Top view (left) and bottom view (right) for one phase of two-phase experimental prototype (1 in×0.75 in×0.226 in)

For the driver circuitry the LTC4440-5 gate driver is used in a conventional cascaded bootstrap configuration. As there are only 3 high-side switches, and silicon MOSFETs are used, not wide-bandgap devices that are highly sensitive to gate drive voltage, the diode voltage drop in this configuration does not negatively impact the circuit performance.

Tab. 3 12-switch ZIV converter prototype components

Component	Value/part number
Input capacitor C_{in}	1×4.7 μF 100 V X7S 1206
First flying capacitor C_{f1}	5×10 μF 50 V 1206 (top) 5×10 μF 35 V 0805 (bottom)
Second flying capacitor C_{f21}, C_{f22}	3×47 μF 25 V 1210 (top) 4×10 μF 35 V 0805 (bottom)
Output capacitor C_{out}	10×47 μF 25 V X5R 1210
*M*1-*M*4	Infineon BSZ025N04LS (40 V, 2.5 mΩ)
*M*51-*M*82	Infineon BSZ017NE2LS5I (25 V, 1.7 mΩ)
Inductors	Coilcraft XEL4030-201 (200 nH, 22 A)
Switching frequency f_{sw}	60 kHz (120 kHz *M*1-*M*4)

The tallest component in the prototype is the inductor at 0.126 in (3.2 mm). On the bottom side of the board, the tallest component is the drivers with a height of 0.04 in (1 mm). Note that on the bottom side of the board 0805 size capacitors (also with a height of 1 mm) are selected. This way the overall height of the converter is minimized, allowing for higher power density to be achieved. Including the board thickness of 0.06 in this gives the overall height of 0.226 in, or 5.74 mm. The MOSFETs selected have a footprint of 3 mm ×3 mm.

Fig. 21 is taken at a 48 V input and 50 A output load. The output voltage (top), $C_{f1\text{-}1}$ ripple voltage (second from bottom), $C_{f21\text{-}1}$ ripple voltage (bottom), and the voltage at $V_{sw21\text{-}1}$ (second from top) are presented.

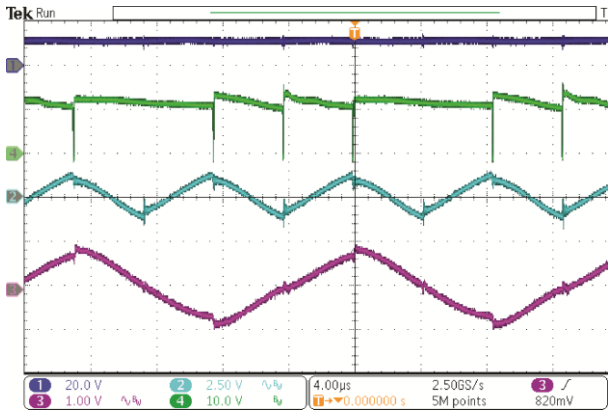

Fig. 21 Experimental prototype waveforms for 48 V input 50 A load

The inductor voltage will be the difference between V_{sw21} and the output voltage. This voltage difference will be a summation of the capacitor ripple voltages, dependent on the circuit state. What should be noted, however, is that the voltage is very small compared to the input or output voltages, allowing for a very small inductor to be used.

For 48 V input the output voltage characteristic of the ZIV converter is presented for the full load operating range in Fig. 22. As expected, based on the analysis, the output voltage decreases linearly in proportion to the load current.

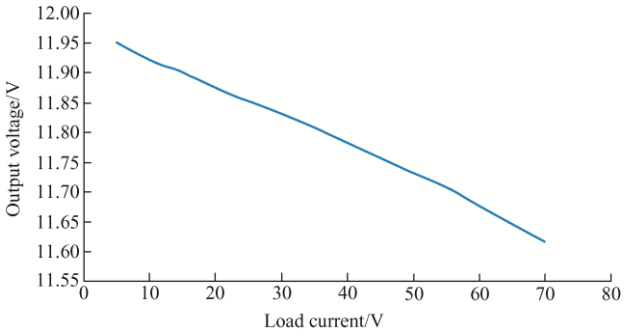

Fig. 22 Measured prototype output voltage characteristic

The efficiency measurements for the ZIV converter for both 48 V and 60 V input are presented in Fig. 23 as measured using a Keithley 2 700 multimeter and Reidon *RSN* series current shunts The maximum output current of the prototype is 70 A. For 48 V input, and 12 V output, the measured full load efficiency is 97.2% including the gate drive loss. The peak efficiency for 48 V input is 99.1%. As compared with Ref. [18] which achieves 12 V/60 A efficiency of 97.2%, the ZIV converter prototype achieves a 12 V 60 A efficiency of 97.8%. For 48 V input, the maximum converter output is 12 V/70 A. The power density of the converter for this output condition is

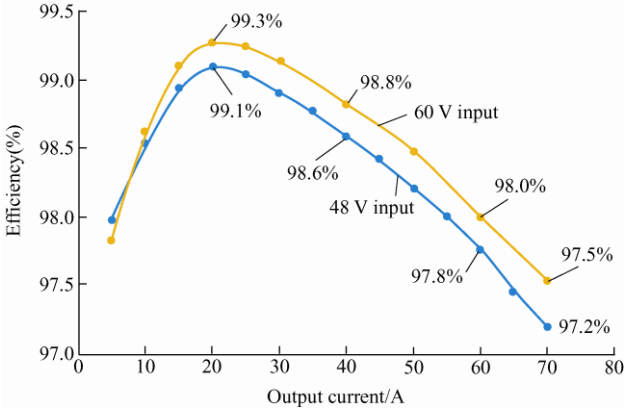

Fig. 23 Measured efficiency for two-phase experimental prototype including gate drive loss

then 2 500 W/in^3. This matches the highest power density yet demonstrated in literature by Ref. [18], while achieving higher overall efficiency.

It should be noted that the maximum load current of 70 A is selected based on thermal considerations. If more powerful cooling is utilized this converter design can output higher current. The saturation current of the selected inductors is 22 A, meaning this two-phase design could theoretically output up to 88 A (just over 1 kW output power) with sufficient cooling.

6 Conclusions

Switched capacitor converters offer significant benefits over many conventional PWM based topologies including reduction in MOSFET voltage stress, and the ability to remove bulky and lossy magnetic components. However, the sensitivity of many SCC topologies to manufacturing tolerances and challenges scaling to differing power levels (through techniques such as paralleling multiple phases) have limited their adoption.

In the ZIV converter topology the critical advantages are maintained, namely reduction in MOSFET voltage stress and ability to use very small magnetic components, without many of the critical drawbacks. The ZIV converter is naturally soft-charged, therefore there is no loss due to charge redistribution and no need to introduce additional inductive elements or complex control to address this. As a conduction loss dominated converter the ZIV converter can be easily paralleled, allowing for scalability to differing power levels. The ZIV converter does not rely on a resonant design, and therefore is not sensitive to component manufacturing tolerances.

The two-phase 12-switch ZIV converter prototype presented in this paper achieves a power density of 2 500 W/in^3, with a peak efficiency above 99% and a full load 12 V/70 A efficiency of 97.2%. In terms of power density, this matches the highest yet demonstrated for 48 V to 12 V conversion by the cascaded resonant converter while achieving higher efficiency.

The reason for this efficiency improvement can be seen by examining the relative current and voltage stresses for the components in the 12-switch ZIV converter as compared with the cascaded resonant converter. Both converter topologies require 2 inductors per phase, however, in the 12-switch ZIV converter both of these inductors carry $1/2I_{out}$ as their *RMS* current. In the cascaded resonant converter, one inductor will carry $1/2I_{out}$ and one inductor will carry the full load current. The ZIV converter requires 12 switches per phase instead of 8, however, all 12 switches in the ZIV converter carry $1/2I_{out}$ when switched on. In the cascaded resonant converter only 8 switches are required, but while 4 of these switches will carry $1/2I_{out}$, 4 of the switches will carry the full load current. Similarly, the current stress of the second stage flying capacitor in the cascaded resonant converter will be equal to the full load current, while in the 12-switch ZIV converter both second stage flying capacitors C_{f21} and C_{f22} carry only $1/2I_{out}$. This means that the overall conduction loss, the dominant source of loss in the converter, is reduced. While the cascaded resonant converter eliminates switching loss due to the resonant operation, the conduction loss dominates the overall loss and therefore the reduced current stress of the ZIV converter allows for higher efficiency to be achieved without needing a resonant based design.

References

[1] D Reusch, S Biswas, Y Zhang. System optimization of a high power density non-isolated intermediate bus converter for 48 V server applications. *IEEE Transactions on Industry Applications*, 2019, 55(2): 1619-1627.

[2] Ericsson PKB 4204B PI datasheet. Mar. 2011. [Online]. Available: https://www.mouser.com/datasheet/2/138/8701-EN_LZT146384_EN_F_PDFV1R7-12146.pdf.

[3] General Electric EBDW025A0B datasheet. Mar. 2016. [Online]. Available: https://library.industrialsolutions.abb.com/publibrary/checkout/EBDW025A0B?TNR=Data%20Sheets%7CEBDW025A0B%7CPDF&filename=EBDW025A0B_v1.29.pdf.

[4] Ericsson BMR457 datasheet. Aug. 2012. [Online]. Available: https://www.mouser.com/ pdfdocs/BMR457.pdf.

[5] Delta Electronics E54SJ12040 datasheet. Oct. 2017. [Online]. Available: http://filecenter.deltaww.com/Products/download/01/ 0102/datasheet/DS_E54SJ12040.pdf.

[6] J Glaser, J Strydom, D Reusch. High power fully regulated eighth-brick DC-DC converter with GaN FETs. *Proceedings of PCIM Europe 2015; International*

Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2015: 1-8.

[7] Vicor PI3546-00-LGIZ evaluation board. Sep. 2018. Available: http://www.vicorpower.com/documents/ datasheets/ ds_pi354x-00.pdf.

[8] D Reusch. High frequency, high power density integrated point of load and bus converters. Virginia: Virginia Polytechnic Institute and State University, 2012.

[9] Vicor BCM48Bx120y300A00 datasheet. Aug. 2016. Available: http://cdn.vicorpower.com/documents/datasheets/BCM48B_ 120_300A00.pdf.

[10] Y Li, X Lyu, D Cao, et al. A 98.55% efficiency switched tank converter for data center application. *IEEE Trans. Ind. Appl.*, 2017, 54(6): 6205-6222.

[11] Vicor IB048E096T48Px Datasheet. Jan. 2018. Available：http://www.vicorpower.com/documents/family_overviews/fo-ibc.pdf.

[12] M H Ahmed, C Fei, F C Lee, et al. 48-V voltage regulator module with pcb winding matrix transformer for future data centers. *IEEE Trans. Ind. Electron.*, 2017, 64(12): 9302-9310.

[13] Z Ye, Y Lei, R C N Pilawa-Podgurski. A resonant switched capacitor based 4-to-1 bus converter achieving 2 180 W/in^3 power density and 98.9% peak efficiency. *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, USA, 2018: 121-126.

[14] Z Ye, Y Lei, R C N Pilawa-Podgurski. A 48-to-12 V cascaded resonant switched-capacitor converter for data centers with 99% peak efficiency and 2 500 W/in^3 power density. *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019: 3-18.

[15] M H Ahmed, M A de Rooij, J Wang. High-power density, 900-W LLC converters for servers using GaN FETs: Toward greater efficiency and power density in 48 V to 6/12 V converters. *IEEE Power Electronics Magazine*，2019，6(1): 40-47.

[16] S V Cheong, H Chung, A Ioinovici. Inductorless DC-to-DC converter with high power density. *IEEE Transactions on Industrial Electronics*, 1994, 41(2): 208-215.

[17] Y Lei, R May, R Pilawa-Podgurski. Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter. *IEEE Transactions on Power Electronics*, 2016，31(1): 770-782.

[18] C K Tse, S C Wong, M H L Chow. On lossless switched capacitor power converters. *IEEE Transactions on Power Electronics*, 1995, 10(3): 286-291.

[19] S Webb, T Liu, Y F Liu. Zero inductor voltage multilevel bus converter. *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018: 2175-2182.

[20] S Webb, Y Liu. 12 switch zero-inudctor voltage converter topology. *2019 IEEE Applied Power Electronics Conference and Exposition (APEC),* Anaheim, CA, USA, 2019: 2189-2196.

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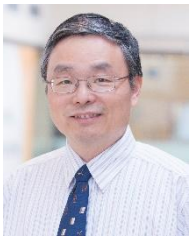

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He has authored around 250 technical papers in the IEEE Transactions and conferences, and holds 35 U.S. patents. He has written a book on "High Frequency MOSFET Gate Drivers: Technologies and Applications", published by IET. He is also a principal contributor for two IEEE standards. He received "Modeling and Control Achievement Award" from IEEE Power Electronics Society in 2017. He received Premier's Research Excellence Award in 2000 in Ontario, Canada. He also received the Award of Excellence in Technology in Nortel in 1997.

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